DOCUMENT-IDENTIFIER: US 4091455 A
TITLE: Input/output maintenance access apparatus

DEPR:
It is seen from the above that the "bad" processor is rendered totally inactive since it is essential that its state be preserved. However, as mentioned previously, the inactive bad processor contains information which will facilitate greatly diagnosis of the reason for failure. For further information regarding the unlocking of processor pairs, reference should be made to the application "Input/Output Processing System Utilizing Locked Processors."

CCOR:
714/25

DOCUMENT-IDENTIFIER: US 5347648 A
TITLE: Ensuring write ordering under writeback cache error conditions

BSPR:
As set out in our Ser. No. 07/547,597, filed Jun. 29, 1990, entitled ERROR TRANSITION MODE FOR MULTI-PROCESSOR SYSTEM, by Rebecca L. Stamm et al., issued on Oct. 13, 1992 as U.S. Pat. No. 5,155,843, a write-back cache may encounter certain error conditions for which data in the cache should be ignored unless that data is owned by the cache. In this case, the cache is put into a state called "Error Transition Mode" (ETM). In ETM, the cache is used as little as possible, and the state of the cache is preserved as much as possible for diagnostic software. In ETM, when a processor, makes a memory request for data not owned by the cache, any data in the cache is ignored, and the data is obtained from main memory; and when the processor makes a memory read request for data owned by the cache, the data is obtained from the cache.

DEPR:
Thus, when the cache controller unit 26 detects uncorrectable errors using the ECC circuits 330 and 331, it enters into Error Transition Mode (ETM). The goals of the cache controller unit 26 operation during ETM are the following: (1) preserve the state of the cache 15 as much as possible for diagnostic software; (2) honor memory management unit 25 references which hit owned blocks in the backup cache 15 since this is the only source of

DOCUMENT-IDENTIFIER: US 4811345 A
TITLE: Methods and apparatus for providing a user oriented microprocessor test interface for a complex, single chip, general purpose central processing unit

DEPR:
The HALT mode is useful for both software debugging and hardware diagnostics since it allows processor 130 to be stopped while preserving its internal state. The HALT mode is defined so that normal operation may resume from the point at which the processor enters the HALT mode. Since all external accesses are completed before the HALT mode is entered, a minimum amount of system logic is required to support the HALT mode.

CCOR:
714/27

DOCUMENT-IDENTIFIER: US 4982402 A
TITLE: Method and apparatus for detecting and correcting errors in a pipelined computer system

DEPR:
FIG. 5 is a flowchart of the control effected by the SCM 44 over the SCD 45.
The SCM control routine begins at block 86 where the faulted CPU clocks are halted. This prevents continued operation of the faulting CPU until such time as its state values have been sampled by the SCM. Moreover, by halting the CPU clocks, the erroneous state conditions are preserved for future analysis.
Control transfers to block 88 where the SCM 44 instructs the SCD 45 to shift the information out of the CPU and into the SCM 44. Once the information has been copied from the CPU 12, control transfers to block 90 where the CPU is reset to its appropriate state. For example, the PC 24 is set to the appropriate value, in the case of asynchronous errors the PC 24 is left at its current state and in the case of synchronous errors the PC 24 is reset to the value corresponding to the instruction which caused the error. Thereafter, control transfers to block 92 where the CPU clocks are restarted and the CPU 12 is allowed to resume execution of its program.

CCOR:
714/15

DOCUMENT-IDENTIFIER: US 5423025 A
TITLE: Error handling mechanism for a controller having a plurality of servers

DEPR:
Each of the servers 104-1, . . . , 104-n, 105, includes local hold logic which is responsive to a local hold signal or the global hold signal to stop and hold state machines within the server at the next available stopping point. This preserves machine state for logout and analysis.

DEPV:
2. The server suffering the error initiates a local hold, in which it will stop and hold its state machines at the next available stopping point. This preserves state machine state for log out and analysis.

CCOR:
714/57

DOCUMENT-IDENTIFIER: US 5559957 A
TITLE: File system for a data storage device having a power fail recovery
mechanism for write/replace operations

DEPR:
As shown in Table I below, if all the flags are set or unset, then the previous
session was not interrupted at the time of the power failure, and the garbage
collection process will be run in its entirety as part of the initialization
procedure. The difference between having all flags set or having all flags
unset is whether the power failure occurred before or after the flags were
cleared after completion of the previous garbage collection session. If,
however, the analysis phase was begun but not completed, the results of that
analysis are discarded and a new analysis phase is commenced. Note that in
this case, the state of the file system 4 is preserved due to the fact that no
events for the interrupted analysis were executed. If the analysis phase was
completed but the execution phase was not begun, the process will then resume
with the execution of events in the event queue 24 written there during the
previous analysis phase. Finally, if the execution phase was begun but not
completed, then execution of the events in the event queue 24 is resumed
starting at that event for which its execution was interrupted. Consequently,
once it is determined during file system initialization whether the previous
garbage collection process was interrupted or not, the initialization proceeds

DOCUMENT-IDENTIFIER: US 5568380 A
TITLE: Shadow register file for instruction rollback

DEPR:
Therefore, the shadow register file for instruction rollback includes checkpoint and retry, interrupt service, programmable constants or improving register select delays. The design integrates the necessary circuitry required to create data paths between a primary and shadow storage device. The dense chip design in which this can be implemented provides cost advantages. The shadow register file allows a fast method for storing a portion of the program state without overly complicated amount of hardware control. At a designated time, the register's files content are preserved in the shadow cells. If at a later time the diagnostic logic of the processor detects an error, the processor can be stopped, reset back to point of the error or the data transferred from the shadow cells back to the memory cells as opposed to the beginning of the instruction sequence and the instructions can be retried again. The need for fault-tolerant features such as instruction rollback rise as new applications for higher reliability systems increases. Among these applications are banking system, medical systems, certain real-time defense systems. In these applications a quick error recovery scheme is essential.
The use of a shadow register file rollback, described above, can help meet the demand for higher reliability.